6. (Original) The method of claim 1 wherein the first material is polysilicon.

7. (Original) The method of claim 1 wherein the second material is oxide.

8. Cancelled.

9. (Currently Amended) ~~The method of claim 1 wherein~~ A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level, the slurry ~~has~~ having a selectivity that falls within an approximate range of 0.9-1.1:1.

10. (Original) The method of claim 2 and further comprising the step of forming a layer of third material on the planarized layer of material.

11. Cancelled.

12. Cancelled.

13. (Currently Amended) The method of claim 10

wherein the planarized layer of material has a first thickness over the wafer upper level, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a ~~value~~ second thickness that is equal to a greater than the first thickness.

14. (Original) The method of claim 1 and further comprising the step of doping the layer of first material prior to forming the layer of second material.

15. (Original) The method of claim 1 wherein the layer of first material is doped polysilicon.

16. (Previously Amended) The method of claim 1 wherein the layer of first material makes an electrical contact with a device on the wafer.

17. (Currently Amended) ~~The method of claim 1 wherein~~ A method for forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material, the second layer of material ~~is~~ being thicker than the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material with a slurry until the layer of second material is substantially all removed from the layer of first material to form the planarized layer of material, the planarized layer of material lying over the wafer upper levels and the wafer lower level.

18. Cancelled.

19. (Previously Amended) The method of claim 22 wherein the first lower level lies above the wafer upper level.

20. (Currently Amended) The method of claim 19

wherein the planarized layer of first material has a first thickness over the wafer upper layer, and

wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a ~~value~~ second thickness that is equal to or greater than the first thickness.

21. (Previously Amended) The method of claim 22 wherein the first material is doped polysilicon.

22. (Currently Amended) A method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; ~~and~~

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and

forming a layer of third material on the planarized layer of first material, the third layer of material lowering a resistance of the first layer of material.

23. (Previously Amended) The method of claim 22 wherein the layer of first material makes an electrical contact with a device on the wafer.

24. (Previously Added) A method of forming a planarized layer of material on a processed wafer, the wafer having a top surface, the top surface having spaced-apart wafer upper levels and a wafer lower level that lies between the wafer upper levels, the wafer upper levels lying above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material;

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of material, the planarized layer of material covering the wafer upper levels and the wafer lower level of the top surface of the wafer; and

selectively etching the planarized layer of material that covers the wafer upper levels and the wafer lower level of the top surface of the wafer.

25. (Previously Added) The method of claim 24 and further comprising the step of forming a layer of third material on the planarized layer of material, the layer of third material and the layer of first material being selectively etched during the selectively etching step.

26. (Cancelled).

27. (Previously Added) The method of claim 24 wherein the layer of first material and the layer of second material are etched with a slurry that etches the layer of first material and the layer of second material at approximately a same rate.

28. (Previously Added) The method of claim 24 wherein all of the layer of second material is removed during the chemically-mechanically polishing step.